Notice of Allowability	Application No.	Applicant(s)	
	09/852,217	ABDALLAH ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *RCE and amendment filed 6/30/04*.

2. ☒ The allowed claim(s) is/are *20,22-25 and 33-144*.

3. ☒ The drawings filed on *23 June 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Eric Coleman
Primary Examiner

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Daniel M. DeVos (Reg. 37,813) on April 18, 2005.

The application has been amended as follows: Replace the all prior versions of claims 38,65, and 127 with the amended version that follows:

38. (amended) A method comprising:
receiving a partial-width packed data instruction, the partial-width packed data instruction specifying locations in a memory of a first packed data operand and a second packed data operand, the partial-width packed data instruction specifying generation of a packed data result, the packed data result having as one or more data elements one or more results of one or more operations performed on one or more pairs of data elements of the first and the second packed data operands, and the packed data result having as one or more remaining data elements one or more predetermined values; and
generating the packed data result responsive to execution of the partial-width packed data instruction.

65. (amended) A method comprising:
receiving a scalar packed data instruction, the scalar packed data instruction specifying locations in a 128-bit logical register file of a processor of a first 128-bit packed data operand and a second 128-bit packed data operand, each of the 128-bit packed data operands including a low-order segment and a high-order segment, and each of the segments including two 32-bit single precision floating point data elements, the instruction specifying generation of a 128-bit packed data result operand, the 128-bit packed data result operand having as a data element a result of an operation performed on a single pair of corresponding least significant data elements of the first and the second 128-bit packed data operands, and the 128-bit packed data operand having as one or more remaining data elements one or more predetermined values; and

generating the 128-bit packed data result operand according to the instruction responsive to execution of the scalar packed data instruction.

127. (amended) A method comprising:
receiving an instruction specifying a first packed data operand and a second packed data operand, the instruction specifying an operation to be performed on only a subset of corresponding pairs of data elements of the first and the second packed data operands;
converting the instruction into one or more micro instructions including a first micro instruction;
receiving from a memory only a portion of the first and the second packed data operands using the first micro instruction;
generating a result by processing the portion of the first and the second packed data operands; and
providing the result to a destination specified by the instruction.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance: The combination of features in the independent claims was not found in the prior art. The prior art comprised storing packed data operands in memory including storing two packed data operands in a single memory location; the prior art also taught operations on the packed data operands including operations on one packed data operand stored in one half of a memory location with another value and storing two packed data operands in one memory location into two separate memory locations for processing. The prior art also taught placing predetermined ones or zeros in a portion of a memory location containing a packed data operand in the "another portion" (the other half) of the same memory location. The claims that have been previously allowed, even with the current amendment these claims are still allowable. The claims include a combination with an instruction that specifies the locations of first packed data operand and second packed data operand and performing operation on the corresponding elements of the

packed data operands and forming a packed data result; and an execution unit or processor or executing the instruction. The claims also include the combination of an instruction that specifies the location of first and second packed operands and accessing the full width operands and dividing the first full width packed operand into first and second portion and the second full width packed data operand into third and fourth portions and determining a partial result of performing an operation on the first and third portions and determining a partial result of processing the second and fourth portions. The claims also include the combination of receiving an instruction specifying a first packed data operand and a second packed data operand, the instruction specifying an operation to be performed on only a subset of corresponding pairs of data elements of the first and second packed data operands converting the instruction into one or more micro instructions including a first microinstruction receiving only a portion of the first and second packed data operands using the first microinstruction and generating a result by processing a portion of the first and second packed data operands providing the result to a destination specified in the instruction. The above combinations were claimed in varying levels of specificity and each independent claim contains at least one combination that was not found in the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674 or (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER